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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,509	10/07/2003	Kuang Chien Hsieh	10322/57	5043

7590 05/11/2005

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EXAMINER	
TRINH, HOA B	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 05/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/680,509	HSIEH ET AL.	
	Examiner	Art Unit	
	Vikki H. Trinh	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *30-53 and 72-101* is/are pending in the application.

4a) Of the above claim(s) *72-77 and 81* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *30-53,78-80 and 82-101* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/07/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group II, claims 30-53 in the reply filed on 03/02/05 is acknowledged.

Newly added claims 72-77, 81, are further withdrawn from consideration, because they direct to different species, which are not part of the original restriction requirement. It is suggested that the claims be canceled.

Claim Objections

2. Claims 33-35, 43, 86-88, 92 are objected to because of the following informalities: In the mentioned claims, the phrase "at least one of amorphous and polystalline" (Ga,P) or (Ga, N), (Ga, As) is vague and ambiguous because it is not clear what applicant has intended to claim. Does (Ga,P) or (Ga, As) or (Ga, N) modify amorphous or polystalline? The examiner in this Office Action interprets that claims to mean either an amorphous or a polystalline notwithstanding (Ga,P) or (Ga, As) or (Ga, N). Appropriate correction is required.

3. Claims 83-101 are objected to under 37 CFR 1.75(c), as being of improper set of claims form for failing to further limit the subject matter of the previous claims. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper form, or rewrite the claim(s). Note that the scope of claims 83-101 are no different from the scope of claims 30-53. Applicant is redundant in drafting claims 83-101

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 30-53, 78-80, 82-101 are rejected under 35 U.S.C. 102(e) as being anticipated by Malik et al. (6,881,644) (hereinafter Malik).

Malik discloses, as to claim 30, a method of bonding two structures (fig. 3D) together, the method comprising depositing low temperature grown semiconductor bonding layers on placing the bonding Layers 54, 52 (fig. 3D) in contact with each other; applying pressure (col. 11, lines 60-65) to the combined structure (fig. 3D), and first and second structures (figs. 2E, 3B, 3D)to form a combined structure (fig. 3D), annealing (col. 7, lines 55-65) the combined structure under conditions sufficient for the bonding Layers 54, 52 to bond the first and second structures together (figs. 2E, 3B, 3D).

As to claim 31, the method of claim 30, further comprising applying the pressure substantially uniformly to the combined structure during annealing (col. 7, lines 55-65).

As to claim 32, the method of claim 30, wherein the annealing of the combined structure (fig. 3D) occurs under conditions sufficient for the bonding layers to form a polycrystalline material (col. 7, lines 55-65).

As to claim 33, the bonding Layer comprises at least one of amorphous and polycrystalline (Ga,As) (col. Col. 8, lines 1-10) and the annealing of the combined structure occurs at a temperature of between about 300C and 500C and for a time sufficient for the bonding Layers to form a (Ga,As) material that is substantially entirely polycrystalline (col. 12, lines 40-50).

As to claim 34, the bonding Layer comprises at least one of amorphous and polycrystalline (Ga,P) and the annealing of the combined structure occurs at a temperature of between about 500C and 70OC and for a time sufficient for the bonding Layers to form a (Ga,P) material that is substantially entirely polycrystalline (col. 12, lines 55-65).

As to claim 35, the bonding Layer (fig. 3D) comprises at least one of amorphous and polycrystalline (Ga,N) and the annealing of the combined structure occurs at a temperature of between about 700C and 900C and for a time sufficient for the bonding Layers to form a (Ga,N) material that is substantially entirely polycrystalline (col. 12, lines 1-15).

As to claim 36, the bonding layers 52, 54 (fig. 3D) are placed in contact with each other without regard for a relative angular orientation of the first and second structures (fig. 3D) to each other.

As to claim 37, at least one of the first and second structures comprises a non-semiconductor substrate (col. 14, lines 30-35).

As to claim 38, the method further comprising fabricating at least one of an electronic and optoelectronic device from the combined structure (col. 8, lines 5-10)

As to claim 39, the annealing of the combined structure occurs under conditions that are not damaging to the first and second structures but are sufficient to form bonds that are strong

enough to survive subsequent processing at temperatures higher than that used during the bonding (col. 7, lines 55-65).

As to claim 40, a bonding interface produced by the annealing is substantially optically transparent to light emitted by the combined structure (col. 12, lines 1-15).

As to claim 41, a bonding interface produced by the annealing is strong enough to be substantially unaffected by processing of the combined structure (col. 12, lines 1-15).

As to claim 42, the deposition deposits between about 3 nm and about 600 nm of material on each of the first and second structures (fig. 3D).

As to claim 43, the deposition deposits at least one of low temperature grown (Ga,As), (Ga,P) and (Ga,N) on at least one of the first and second structures. (col. 14, lines 53-67)

As to claim 44, the method includes selecting a composition of the bonding layer such that an amorphous layer is deposited on at least one of the first and second structures. (col. 14, lines 53-60).

As to claim 45, the annealing of the combined structure occurs under conditions sufficient for the bonding layers to form a polycrystalline material from the amorphous layer.

As to claim 46, the method includes selecting a composition of the bonding Layer such that a polycrystalline semiconductor Layer is deposited on at least one of the first and second structures (col. 8, lines 1-10).

As to claim 47, the annealing of the combined structure occurs under conditions sufficient for the bonding Layers to recrystallize into a polycrystalline material (col. 7, lines 55-65, col. 8, lines 1-10).

As to claim 48, the annealing occurs at temperatures of at most about 800C (col. 12, lines 45-50).

As to claim 49, the bonding layer comprises a compound semiconductor (col. 8, lines 1-10).

As to claim 50, the method includes doping the bonding layer with Si (col. 8, lines 1-15).

As to claim 51, the step of doping the bonding Layer with a dopant that helps to control morphology of the compound semiconductor (col. 8, lines 1-15).

As to claim 52, Ga-rich low temperature grown semiconductor bonding Layers are deposited (col. 8, lines 1-10).

As to claim 53, the bonding Layer is deposited by molecular beam epitaxy (MBE) at a temperature of at most about 100C (col. 12, lines 15-20).

As to claims 83-101, the examiner has stated in the above that claims 83-101 are redundant of claims 30-53, hence claims 83-101 fall with the rejected of claims 30-53.

As to claim 78, at least one of the first and second structures comprises a semi-insulating substrate (fig. 3D).

As to claim 79, the structures include an insulator (fig. 3D).

As to claim 80, the structures are a "pseudomorphic" structure (fig. 3D).

As to claim 82, the bonding layer is devoid of polymers, metal, and ceramics (col. 8, lines 1-10).

Conclusion

Ghyselen et al. (6,867,067) discloses a method of bonding two structures together having substrates, bonding layers.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Vikki Trinh whose telephone number is (571) 272-1719. The Examiner can normally be reached from Monday-Friday, 9:00 AM - 5:30 PM Eastern Time. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Wael Fahmy, can be reached at (571) 272-1705. The office fax number is 703-872-9306.

Any request for information regarding to the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Also, status information for published applications may be obtained from either Private PAIR or Public Pair. In addition, status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. If you have questions pertaining to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy. Requests

to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

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PRIMARY EXAMINER